

The Examiner's attention is also directed to several relevant sections of *Ho et al.* Specifically, in column 1, lines 13-15, *Ho et al.* indicates that the invention relates to an automatically configuring memory subsystem for use with a computer wherein a pluggable memory cards are modules of any memory size maybe plugged into any of the allocated sockets of the computer. See also column 3, lines 30-35, wherein it indicates that the module sockets 14A, 14B may be located, for instance, in a computer chassis having a number of expansion memory sockets. Nowhere does *Ho et al.* indicate that the entire memory subsystem is provided on a printed wiring board or a memory board as recited in the claims of the present application. Furthermore, *Ho et al.* indicates in column 4, lines 26-28, that local address bus 30 and local data bus 32 are connected to the subsystem 10 from the computer's CPU. This further suggests that the subsystem 10 is not a separate printed wiring board or memory board as suggested by the Examiner.

Accordingly, the Examiner has provided no additional evidence other than reciting the Examiner's understanding. Given that 35 U.S.C. §102(b) places a burden on the Examiner to show that the claimed invention is taught in the prior art, the Examiner has clearly not met this burden. All teachings of *Ho et al.* indicate or suggest that the module sockets 14A, 14B are part of the computer chassis, and are not on a separate memory board.


Accordingly, the Examiner is requested to withdraw the rejection.

In the event that there are any questions concerning this Response, or the application in general, the Examiner respectfully urged to telephone the undersigned attorney so that prosecution of the application may be expedited.

Respectfully submitted,

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Date: September 28, 2005

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